Journal of Communications Technology, Electronics and Computer Science, Issue 12, 2017
ISSN 2457-905X

Low Power, Area Efficient Dynamic Voltage Comparator With Reduced Activity Factor

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***Abstract*—This paper introduces the design of dynamic voltage comparator with reduced activity factor for low voltage and low power operation. An analysis of CMOS circuit power consumption is presented along with implication of activity factor on power consumption. A new architecture based on theoretical analysis for a dynamic comparator is proposed. The proposed comparator has a reduced activity factor and thus it consumes less power and it also has reduced transistor count over the design of double tail dynamic comparator which gives the area efficiency. The proposed design compares small input differential voltages efficiently with low power consumption. All circuit designs are simulated in Tanner tools V16 with 90nm CMOS technology. Simulation result shows that proposed design has less active and standby power consumption.**

Keywords—dynamic comparator; double tail comparator; activity factor; input differential voltage(ΔV_{in})

I. INTRODUCTION

Comparators are those circuits which found wide applications in flash type ADC, zero crossing detectors, null detectors. It compares two input voltages available at it's input and gives the output. A dynamic comparator has two outputs, from the pattern of output bits one can know which input is high. A dynamic comparator is different from op-amp based comparator. Since dynamic comparator circuits are controlled by clock signal so, it is also called as clocked regenerative comparators [14] which compare inputs only when the high clock pulse is applied.

Till date many researchers had proposed different circuit architectures of dynamic comparator for power, speed and area efficiency. Techniques for low power design includes supply boosting technique [2], body driven transistor technique [5], charge sharing technique, current mode design. Each of these technique has its own pros and cons such as supply boosting technique presented in [2] increases voltage magnitude to avoid switching problems but it introduces reliability issue such as oxide failure. Body driven transistor technique removes the requirement of threshold voltage [14] but it suffer from low trans-conductance issue which add more delay and it require special fabrication process.

A circuit of conventional dynamic comparator given in [14] consist of a single stage with a cross coupled inverter pair (latch). The analysis given in [1] shows that, speed and power of the latch is affected by various practical limitations. The charging and discharging of node capacitances of the CMOS circuits dominates to overall delay and power consumption [11]. To discharge node voltage faster, the discharging current should be high enough. The double tail design proposed in [14] has two large size tail transistors connected to supply rails which handle high charging and discharging current for delay optimization. As many designs proposed for power and speed optimization, new problems are introduced such as output swing problem, lower trans-conductance, low sensitivity and many more such as, it is found that, for low supply voltage if the input differential voltage (ΔV_{in}) is less, then overall power consumption of circuit becomes high. Likewise, they are unable to compare small ΔV_{in} in low supply voltage (V_{dd}).

To address output swing problem domino logic based comparator design were proposed in [10], the design presented in [14] avoids the sensitivity issue. But those designs are not area efficient. By modifying architecture presented in [14] a new architecture for dynamic comparator can be proposed by removing cross coupled inverter pair [1] and by reducing activity factor to save power, area and to address low sensitivity problem for small ΔV_{in}.

The rest of paper is organized as; section II give an introduction to the dynamic comparator operation with pros and cons of each design. An analysis for the MOSFET and dynamic comparator power consumption is discussed in section III. Section IV describes the proposed methodology and design. Simulation results are listed in section V and section VI concludes the paper.

II. BACKGROUND

A dynamic comparator may be a single stage or multistage [14] controlled by the input clock. Based on the clock magnitude it works in two phases, one is a reset phase (when clock = 0, standby mode) and other is a comparison phase (when clock = 1, active mode). The output of this dynamic comparator generated in two phases, latching phase and regeneration phase. Fig. 1. shows the output waveform of a

dynamic comparator [14] which indicates the output generation phases.

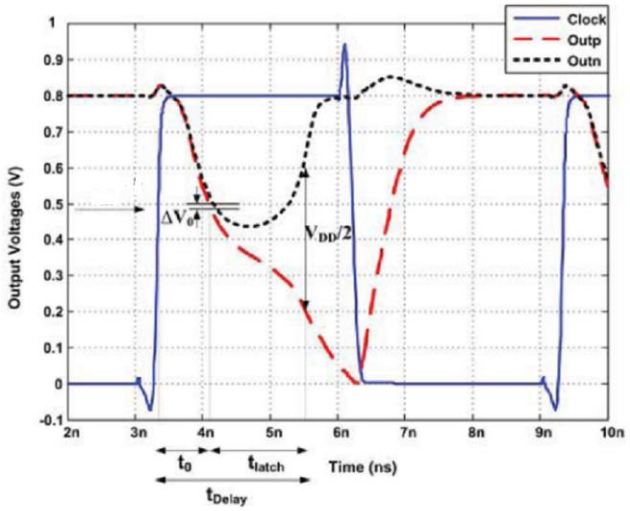

Fig. 1. Transient simulation waveform of the conventional dynamic comparator represents output waveform generation

A. Conventional Dynamic Comparator

A schematic diagram of conventional dynamic comparator is shown in fig. 2. The working of this comparator is as, in a reset phase (clock = 0; N_5 = OFF; P_3, P_4 = ON). Both the output capacitive nodes (O_p and O_n) are charged to V_{dd} through P_3 and P_4. In comparison phase (clock = 1; N_5 = ON; P_3, P_4 = OFF) the output nodes O_p and O_n start discharging through path X_1 and Y_1 respectively. If $I_p > I_n$ then the channel formed by a transistor N_4 will stronger (will offer low resistance) than channel of N_3, so path X_1 will offer the low resistance than path Y_1, thus node O_p discharge faster than O_n. As node O_p discharged to V_{TH} of P_1 earlier than node O_n, P_1 turns ON and pull the node O_n to V_{dd}. The cross coupled inverter pair formed by P_1, N_1 and P_2, N_2 pull down node O_p.

This circuit architecture has the advantage of a low power consumption and small area requirement [14] as transistor count is less. But at the other side this design requires more delay to generate output, it requires high supply voltage (1.5 V) and give the high power consumption for a smaller ΔV_{in}, also this design suffers from the low sensitivity issue. Transistor N_5 share the discharging current from both paths X_1 and Y_1 thus the channel conductivity of N_5 should high for a proper delay time. This lead to use wider channel and hence large sized transistor is required [14] which will add more area.

B. Conventional Dynamic Double Tail Comparator

Fig. 3. Shows the schematic diagram of conventional dynamic double tail comparator [14] which consist of two stages, input and output stage. Transistors P_4, P_5, N_3, N_4, N_5 forms the input stage and P_1, P_2, P_3, N_1, N_2, N_6, N_7 forms the output stage. In the reset phase (clock = 0; P_1, N_5 = OFF; P_4, P_5 = ON) node f_p and f_n are charged to V_{dd} lead to N_6 and N_7 turn ON. Both N_6 and N_7 discharges output nodes O_p and O_n to ground. Whereas in comparison phase (clock = 1; P_1, N_5 = ON; P_4, P_5 = OFF) if $I_p > I_n$ then the path X_{11} will offer low resistance than Y_{11} which discharge node f_p faster than node f_n. A discharged node f_p turn OFF N_7 which charges O_p to V_{dd} and further on latch action pull O_n to ground.

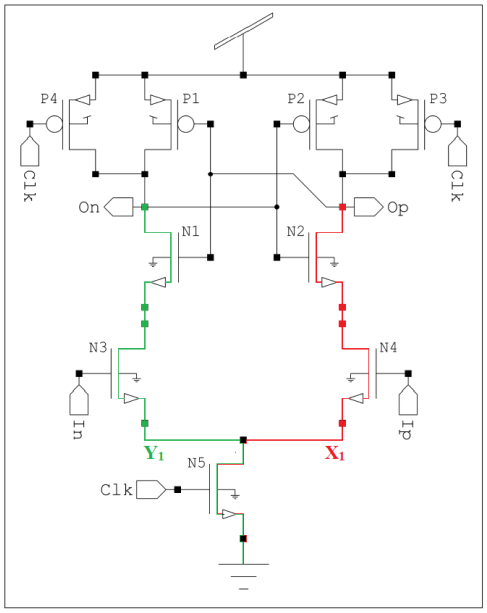

Fig. 2. Schematic diagram of the conventional dynamic comparator

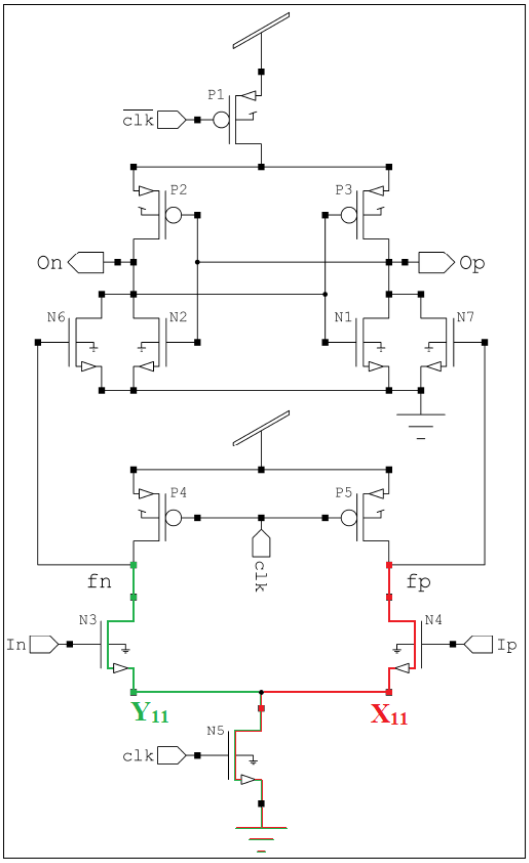

Fig. 3. Schematic diagram of conventional dynamic double tail comparator

This design has ability to operate on small supply voltage (1 to 1.2V) but it is found that the overall delay of this comparator depends on magnitude of ΔV_{in} and it requires large sized tail transistors also it consumes more power for comparing analog signals.

C. Optimized Dynamic Double Tail Comparator

The schematic diagram of optimized dynamic double tail comparator [14] is shown in fig. 4. The operation of this comparator is as follows. In reset phase (clk = 0; P_1, N_9 = OFF; P_6, P_7 = ON) node f_p and f_n charged to V_{dd} through P_6 and P_7 which turn ON N_3, N_4 and both the output nodes discharged to ground through N_3 and N_4. During a comparison phase (clk = 1; P_1,N_9 = ON; P_6, P_7 = OFF) both the output nodes keep discharging also node f_p and f_n start discharging through path X_{11} and Y_{11} respectively. If $I_p > I_n$ then path X_{11} will offer low resistance than Y_{11} as channel of transistor N_6 becomes stronger than N_5. So, node f_p will discharge faster than f_n and it will turn OFF N_3. Afterward O_p charged to V_{dd} and O_n discharged to logic 0 due to cross coupled latch action. The transistors N_7 and N_8 are used to avoid static power consumption [14].

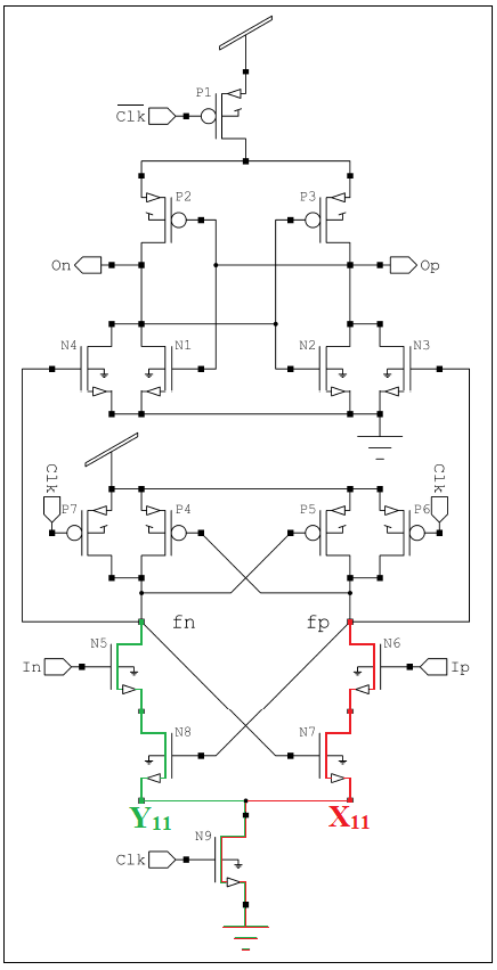

Fig. 4. Schematic diagram of optimized dynamic double tail comparator

Although this circuit has advantages of low voltage operation (1 to 1.2V) but it suffers from some limitations like, it gives excess power dissipation for comparing analog signals as well as for small $\Delta V_{in.}$

III. CMOS Circuit Analysis

A. Analysis for CMOS Power Consumption

An analysis given in [11] give the instantaneous power consumed by MOSFET as follows,

$$P(t) = I(t) \times V(t) \tag{1}$$

Total energy consumed over some time interval is given by integrating instantaneous power consumption. By integrating equation (1),

$$E = \int_0^T P(t)dt \tag{2}$$

Average power consumed over interval (0 to T) is given by,

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T P(t)dt \tag{3}$$

In CMOS circuits average power consumption is based on two components [11] given as follows,

1. **Static power consumption** - due to sub-threshold leakage through OFF transistor, gate leakage through gate dielectric and junction leakage from source/drain diffusion.
2. **Dynamic power consumption** - due to charging and discharging of load capacitances (nodes) and short circuit current flow.

A static power consumption can be reduced by connecting less number of transistors to supply rails, such technique is adopted in double tail comparator [14]. Also dynamic power consumption is mainly caused due to transistor switching (node charging and discharging) given as,

$$P_{switching} = \alpha C_L V_{DD}^2 f \tag{4}$$

Equation (4) clear that, to reduce switching power, operating frequency (f), load capacitance (C_L), supply voltage (V_{DD}) and activity factor (α) must be reduced. Activity factor is the probability that circuit node will have transition from logic 0 to logic 1.

B. Analysis for Dynamic Comparator Speed

As shown in fig. 1. the total delay of dynamic comparator is consist of two delays,

$$T_{delay} = T_0 + T_{latch} \tag{4}$$

T_0 is the time required to discharge node f_p or f_n to voltage such that one of the nMOS connect to it will turn off. T_0 delay

occurs in input stage of comparator. T_{latch} is the time required to regenerate output voltage at node O_p or O_n. T_0 can be given as [11],

$$T_0 = \frac{C_L V_{th}}{I_2} \cong 2\frac{C_L V_{th}}{I_2} \quad (5)$$

I_2 is the current through transistor N_9 shown in fig. 4. Which is discharge current of node f_p and f_n. Thus by increasing discharge speed of the nodes T_0 can be reduced. T_{latch} is given as [11],

$$T_{latch} = \frac{C_L}{g_{m,eff}} \cdot ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) \quad (6)$$

$g_{m,eff}$ is the effective trans-conductance, to increase $g_{m,eff}$ the channel should have large current for small gate voltage. ΔV_o is a voltage difference between node f_n and f_p which contribute to latch delay. From fig. 4. Transistors P_4 and P_5 are used to provide large ΔV_o.

IV. Proposed Design

A. Proposed Methodology

Apart from doing any technological modifications, a significant optimization can be done by modifying the conventional design architectures. As stated in [14], "input differential voltage and output differential voltage contributes to power consumption and delay." As the inputs are real time so it is hard to maintain difference between them or extra circuitry will required, so it is worthy to maintain difference between outputs produced (between f_p and f_n) in input stage of dynamic double tail comparator. To achieve large ΔV_o between f_p and f_n two topologies can be proposed,

1. Discharge node f_p and charge node f_n (used in double tail comparator [12] [14], but it increases activity factor and hence power consumption)
2. Discharging of node f_p will oppose discharging of node f_n so that node f_n will not completely discharged (proposed methodology)

An analysis of cross coupled inverter pair given in [1] clear that latch has some practical limitations on speed and power consumption, so proposed design removes latch from output stage.

B. Node Discharging and Activity Factor Reduction

As shown in fig. 5, in conventional node discharge method, Out_n discharges to 1.1V and again charge to 1.2V. This frequent discharging and charging of the capacitive node lead to increase in an activity factor. Fig. 6. shows the waveforms for the proposed topology in which the Out_n node discharge to 0.7V gradually without frequent discharge. Thus in proposed topology the activity factor is reduced. The voltage level of a node Out_n is decreased during the clock=1 though it is able to drive output stage of comparator. From fig. 7. the output stage of the proposed comparator is implemented without cross coupled inverter pairs which again reduces activity factor and hence power consumption.

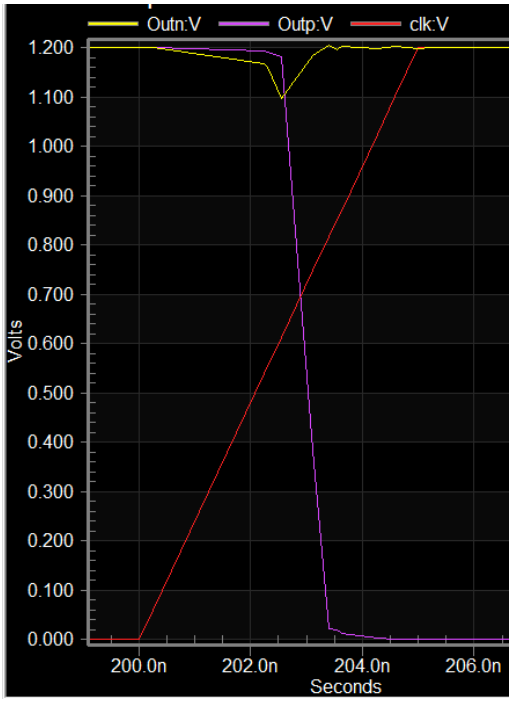

Fig. 5. Transient simulation waveform for conventional node discharge topology

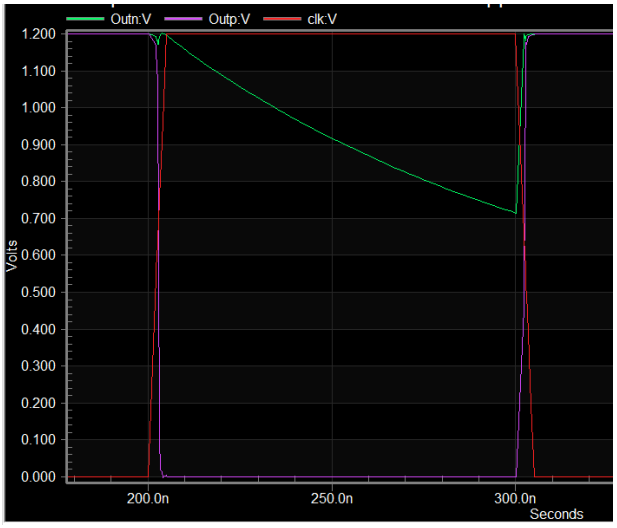

Fig. 6. Transient simulation waveform for proposed node discharge topology

C. Proposed Design

Fig. 7. shows the schematic design of proposed dynamic comparator with modified node discharge methodology at input stage and the output stage is implemented without cross

coupled inverter pair. The working of this circuit is as, in reset phase (clock = 0; N_9 = OFF; P_3, P_4 = ON) both nodes f_p and f_n are charged to V_{dd} through P_3 and P_4 which lead to turn ON N_1, N_2, and thus output nodes O_p, O_n are discharged to ground. During comparison phase (clock = 1; N_9 = ON; P_3, P_4 = OFF). The pre-charged f_p and f_n starts discharge. If $I_p > I_n$ then path X_{11} will offer low resistance than path Y_{11}. For a instance f_p will discharge faster than f_n such that $Vf_p < Vf_n$ so that channel of transistor N_5 will made weaker by discharged f_p. At certain stage, f_p will completely discharged and will turn OFF N_5 completely and still f_p is charged to V_{th} of N_1 which keep O_n to logic 0. A discharged node f_p will turn OFF N_2 and O_p will charge to logic 1. Transistor N_3 and N_4 are used to avoid glitches on output nodes for smaller ΔV_o.

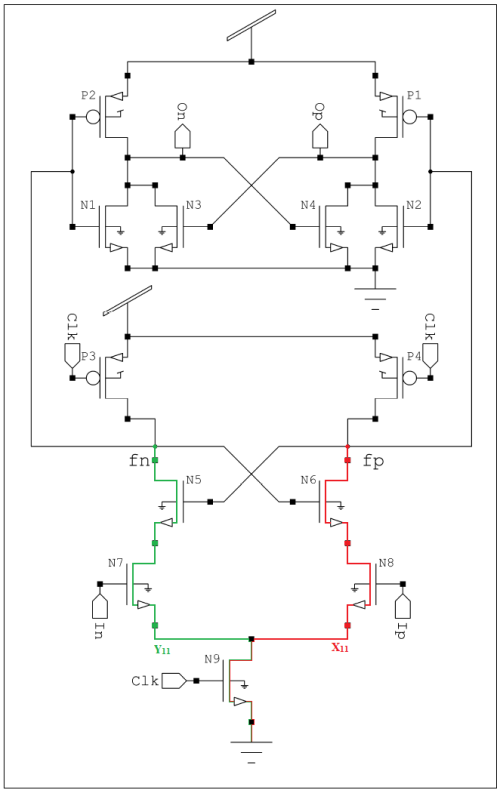

Fig. 7. Schematic diagram of proposed dynamic comparator

V. Simulation Results

The all conventional and proposed circuits are simulated in Tanner tools V16 with 90nm CMOS technology with simulation parameters as, V_{dd} = 1.2V (DC); F = 500MHz; I_p = 1.2V (AC), 50KHz, delay = 0v and I_n = 1.2V (AC); 50KHz; delay = 5µs. The transient simulation set for period of 20µs such that analysis for single cycle with all conditions of ΔV_{in} will be verified. The respective simulation waveforms are shown in fig. 9. which verifies all input conditions. The post simulation results shows that proposed comparator consumes less power in active as well as standby mode. Fi9. 8. shows the transient simulation waveforms for the DC input signal, for I_P = 1.1V and I_n = 1V the outputs are O_p = 1 and O_n = 0.

Table I depicts the active and standby power consumption for various dynamic comparator topologies. The proposed design architecture consumes much less power as compared to comparator presented in [14]. Also design presented in [12] has approximately same standby power consumption as compared to proposed design but it requires more power in active phase. Table II confirms that, the proposed design has less transistor count as compared to DTC and has same number of transistors as compared to the design proposed in [12] with advantage of sensitivity. The proposed design has lowest power consumption for ΔV_{in} = 0, which prove that, the proposed design is a good choice for null detector also.

TABLE I. POWER CONSUMPTION COMPARISON

Design	Active Power (µW)	Standby power (nW)
Dynamic comparator [12]	4.4455	57.9323
Optimized DTC [14]	27.5131	76.0017
Proposed Dynamic Comparator	1.2541	57.6217

TABLE II. TRANSISTOR COUNT AND SENSITIVITY COMPARISON

Design	Transistor Count	Sensitivity (mV)
Dynamic comparator [12]	13	5
Optimized DTC [14]	18	2
Proposed Dynamic comparator	13	2

TABLE III. IMPACT OF ΔV_{in} ON POWER CONSUMPTION

Design	ΔVin (mV)	Power Consumption (µW)
conventional dynamic comparator [14]	200	4.71
	50	4.64
	10	67.80
	0	67.60
conv. DTC [14]	200	1.86
	50	1.22
	10	13.92
	0	25.38
optimized DTC [14]	200	13.17
	50	35.21
	10	13.42
	0	71.91
dynamic comparator [12]	200	64.38
	50	68.25
	10	104.25
	0	150.04
proposed dynamic comparator	200	4.55
	50	11.11
	10	20.62
	0	1.93

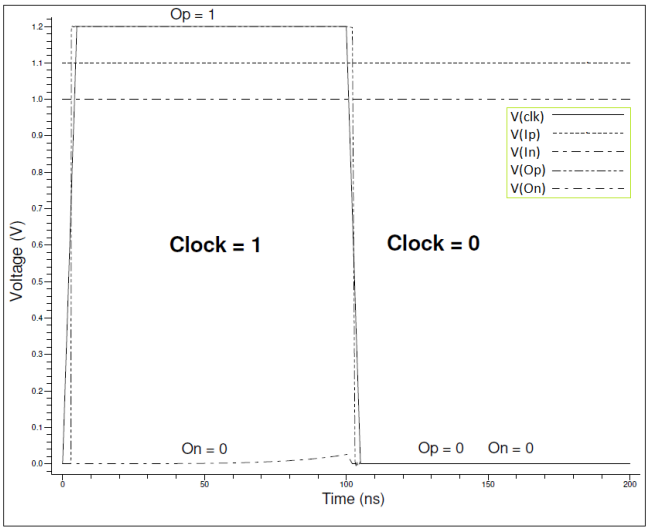

Fig. 8. Transient simulation waveform for DC input signal which verifies working of the proposed comparator

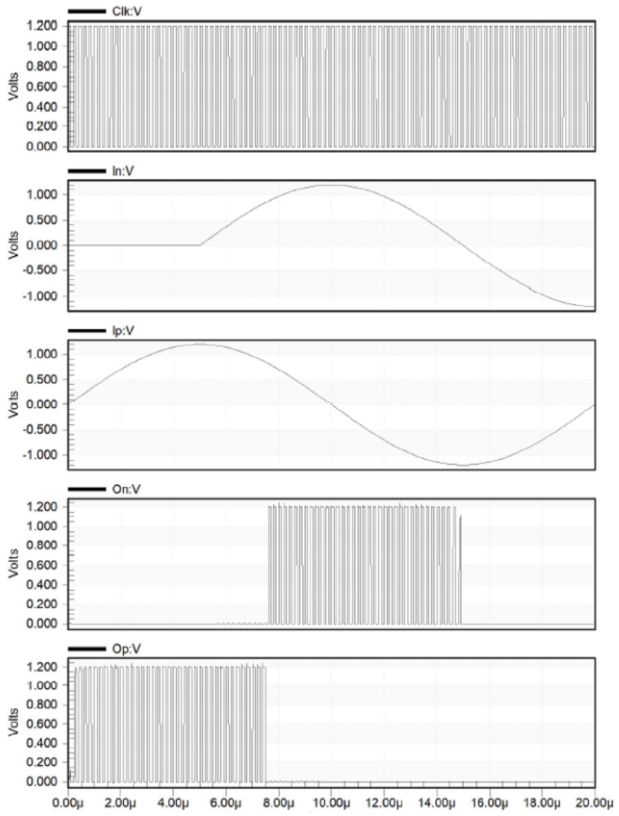

Fig. 9. Transient simulation waveforms for proposed dynamic comparator

VI. Conclusion

In this paper, analysis for CMOS power consumption were derived. From analysis it is shown that power consumption in CMOS circuits depends on activity factor, operating frequency and load capacitance. Also a new modified architecture without latch and reduced activity factor were presented which gives promising power optimization for small ΔV_{in} and ΔV_0 also consumes much less power in active as well as in standby mode.

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