A Quantitative Approach of Reversible Logic Gates in QCA

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***Abstract*—Quantum Dot Cellular Automata (QCA) is an eminent nanotechnology and solution of Complementary Metal Oxide Semiconductor (CMOS) for its computation and transformation procedure. It is attractive for its size, faster speed, highly scalable, feature, low power consumption and higher switching frequency compared to CMOS technology. Reversible logic has many factual operation in QCA as well as VLSI design, nanotechnology, digital signal processing (DSP). This paper presents a systematic design of reversible gate based on QCA. A modified pattern of Fredkin gate, MCL gate and a new scheme of URG gate, BJN gate is proposed in this paper. For design and verification QCADesigner, a widely used simulation tool is employed. The proposed circuits can be used in erecting of nano scale, low power information processing system and modeling complex computing systems.**

***Keywords*—QCA; Fredkin gate; MCL gate; URG gate; BJN gate.**

I. Introduction

Nanotechnology provides new dimensions for computing for its authentic attribute like power consumption, high device density and speed. Quantum dot Cellular Automata (QCA) [1, 2] pledge aforementioned components among auspicious technologies. It has been recently perceived as one of the dominant six rising technologies with stout applications in future computing [3, 4] for its lower power consumption, higher scale integration, high speed and higher switching frequency in various computational operations [5, 6]. The reversible logic circuits construct the vital architecture of quantum computers and generally used in power derogation having the operation as quantum computing, DNA computing, low power CMOS design, communication, computer graphics and cryptography [7, 8, 9, 10]. Energy loss is an imperative thought in constructing a digital system. Energy dissipation due to information fall in high technology circuits and systems constructed using irreversible logic circuit was demonstrated by R. Landauer. Landauer's principle presents that the loss of one bit of information lost, will dissipate *kTln (2)* joules of energy, where *k* is the Boltzmann's constant and T is operating temperature in Kelvin [11]. Later, Bennett manifest that to elude *k*Tln2 joules of energy dissipation in a circuit, it must be fabricated from reversible circuits [12]. In reversible logic circuits information lose is not feasible so it is preferred to design combinational circuit. In this paper, the modified architecture of Fredkin gate, MCL gate and new design of URG gate, BJN gate is presented with the simulation outcomes of each individual scheme.

II. Reversible Logic Gates

A gate is called reversible if there is a one to one correspondence between its output and input assignments. In reversible logic gate, the number of inputs are identical to number the outputs and engender distinct set of output vector for each set of input vector. A reversible circuit should be composed using a nominal number of reversible gates. Some of the fundamental reversible gates are:

A. FREDKIN Gate

Fredkin gate also known as CSWAP gate is a 3x3 gate.The outputs are P=A, Q=A'B+AC, R=AB+A'C.

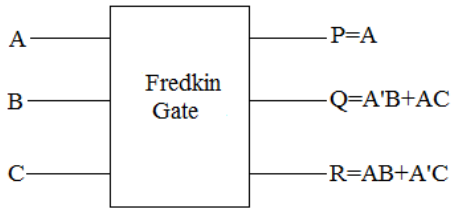


Fig. 1. Fredkin gate.

TABLE I. TRUTH TABLE OF FREDKIN GATE

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

B. MCL Gate

Multiply Complements Logic (MCL) is a 3x3 gate. The outputs are P= B'C', Q = A'B', R = A.

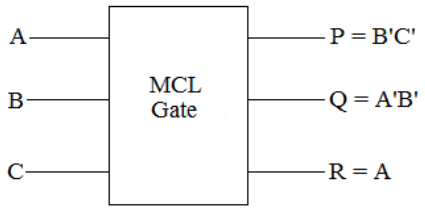


Fig. 2. MCL gate.

TABLE II. TRUTH TABLE OF MCL GATE

Input			Output		
A	B	C	P	Q	R
0	0	0	1	1	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	1	0	1
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	0	0	1

C. URG Gate

Universal Reversible logic gate (URG) is a 3x3 gate. The outputs are P= (A+B)⊕C, Q=B, R= AB⊕C.

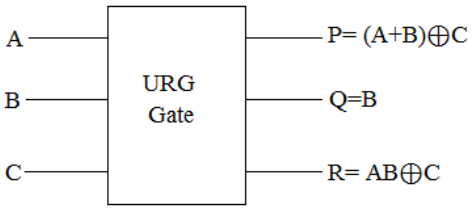


Fig. 3. URG gate

TABLE III. TRUTH TABLE OF URG GATE

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	0	1
1	1	0	1	1	1
1	1	1	0	1	0

D. BJN Gate

BJN is a 3x3 gate. The outputs are P = A, Q = B, R = (A+B)⊕C.

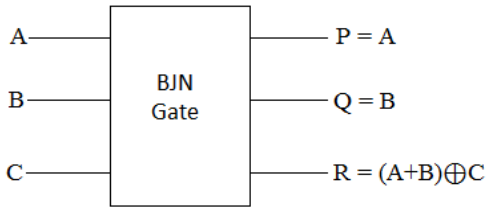


Fig. 4. BJN gate.

TABLE IV. TRUTH TABLE OF BJN GATE

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	1	0

III. TECHNICAL IMPLEMENTATION

Several approximate simulators are employed such as the nonlinear approximation and bistable simulation approaches for testing the design level. But these approaches are iterative, so it cannot produce the actual results. Finally QCA Designer 2.0.3 is chosen and this simulation engine is illustrated [13]. QCA Designer is a widely used simulation engine for a model and verification of QCA based circuits. The correctness of the circuits are evaluated by the simulation tool of QCA Designer 2.0.3 [14]. The technical presentation are shown below.

A. Fredkin Gate

The quantum implementation of fredkin gate shown in Fig. 5 has been proposed by various authors [15].

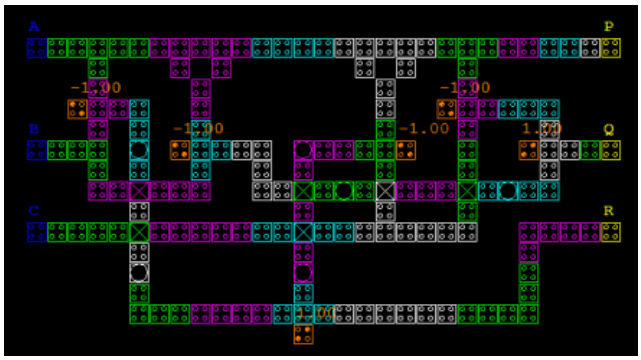


Fig. 5. Structure of the Fredkin gate in QCA.

The designed fredkin gate shown in Fig. 6. The input vector are I (A, B, C) and output vector are O (P, Q, R). The output expression are P=A, Q=A'B+AC and R=AB+A'C. It has been designed in terms of cell count and complexity. The proposed circuit requires less number of cell compared to others.

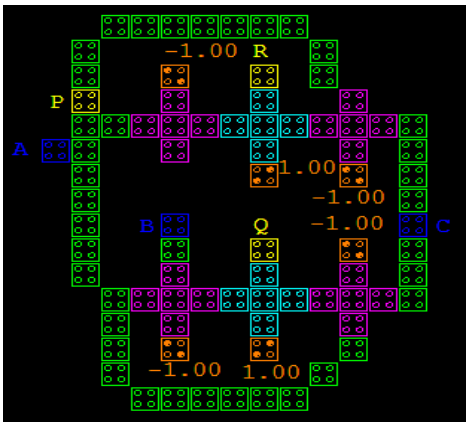


Fig. 6. Structure of the proposed Fredkin gate in QCA.

B. MCL Gate

The QCA implementation of mcl gate has been proposed by various authors [16] and shown in Fig. 7. Here, the inputs are denoted as A, B, C and the outputs are P, Q, R.

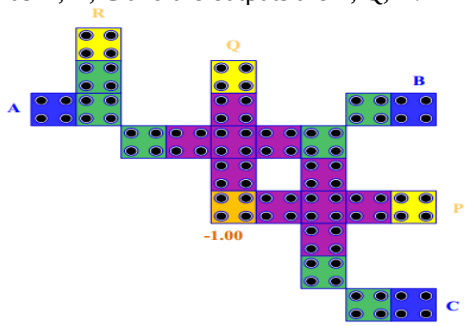


Fig. 7. Structure of the MCL gate in QCA.

The proposed mcl gate shown in Fig. 8. The input vector I (A, B, C) and output vector O (P, Q, R). The output defined as P= B'C', Q = A'B', R = A.

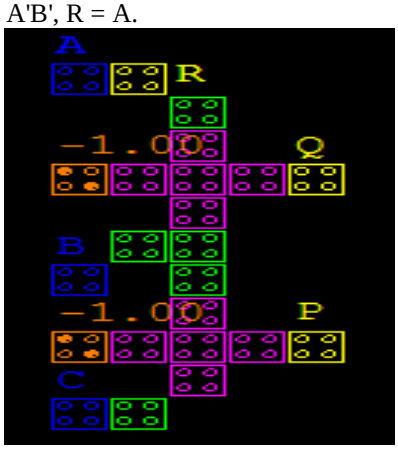


Fig. 8. Structure of the proposed MCL gate in QCA.

C. URG Gate

The implementation of urg gate shown Fig. 9 where the input and output vector denoted as I (A, B, C) and O (P, Q, R).

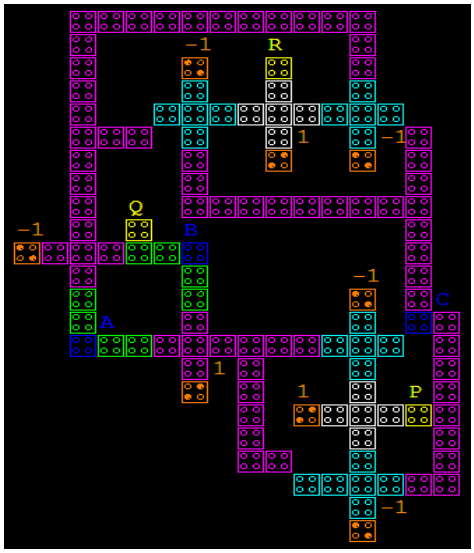


Fig. 9. Structure of the URG gate in QCA.

D. BJN Gate

The qca implemented bjn gate shown in Fig. 10. The input vector is defined as I (A, B, C) and output vector is O (P, Q, R).

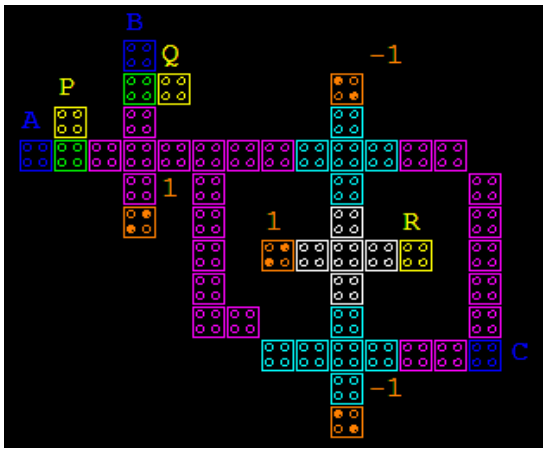


Fig. 10. Structure of the BJN gate in QCA.

Clock zones

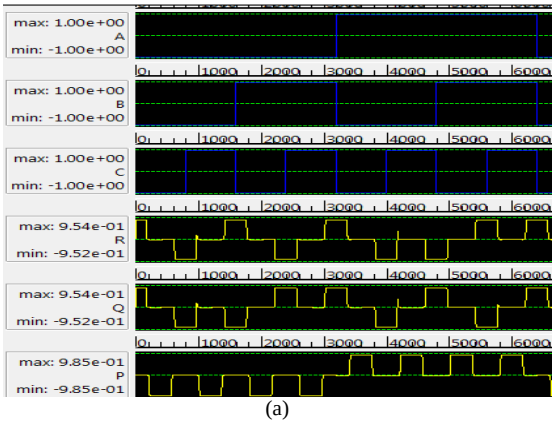
IV. Simulation and Results

Our proposed logic gates were functionally simulated using QCA Designer 2.0.3. We use successive criterions in the bistable approximation which are the default values in QCADesigner. These parameters are shown in table 5.

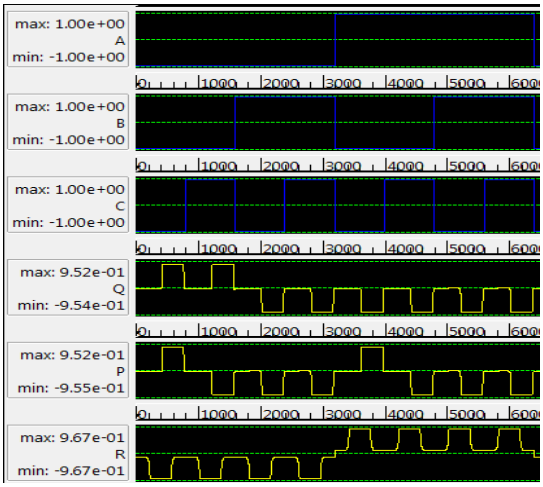
TABLE V. PARAMETERS OF BISTABLE APPROXIMATION

cell size	18nm
dot diameter	5.000
number of samples	12800
radius of effect	65.000000nm
convergence tolerance	0.001000
relative permittivity	12.900000
clock shift	0
clock amplitude factor	2.000000
layer separation	11.500000
clock high	9.800000e–022 J
clock low	3.800000e–023 J
upper threshold [1]	0.500
lower threshold [0]	-0.500
maximum iterations per sample	100

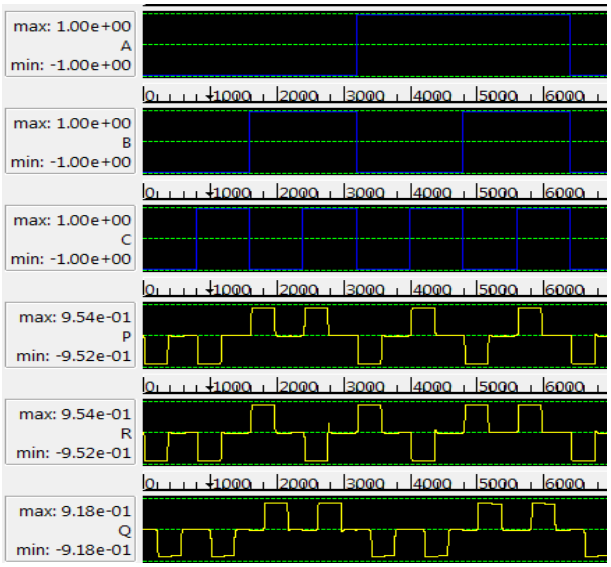
The simulated results of reversible gates are shown below:



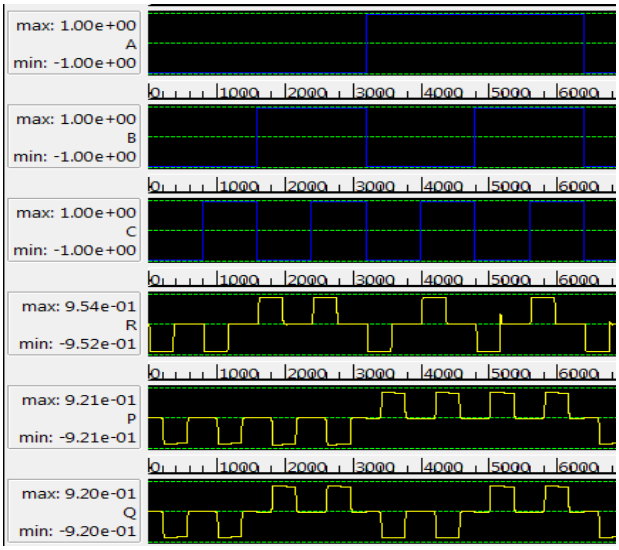
(a)



(b)



(c)



(d)

Fig. 11. Simulated waveforms in QCADesiner (a) Fredkin gate (b) MCL gate (c) URG gate (d) BJN gate.

TABLE VI. PERFORMANCE COMPARISON OF PROPOSED LAYOUT

Reversible Gate	Parameter		
	Number of cells	*Area(μm^2)*	*Clock delay*
Fredkin gate	187	0.19	2.00
Proposed Fredkin gate	81	0.09	0.75
MCL gate	24	0.03	0.50
Proposed MCL gate	23	0.02	0.50
URG gate	122	0.15	1.00
BJN gate	51	0.07	1.00

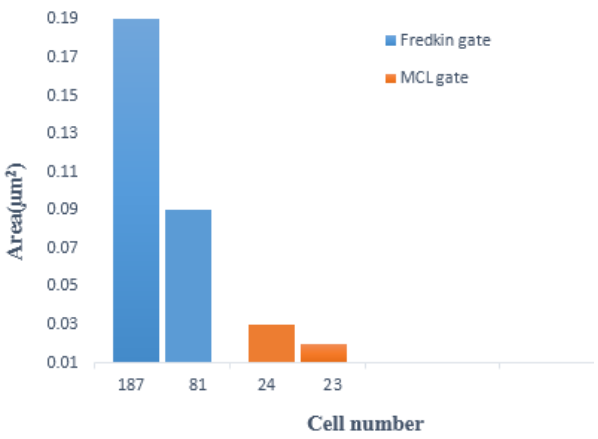


Fig. 12. Comparative figures for area and cell of proposed fredkin and mcl gate.

V. Conclusion

This paper explores a novel scheme of Fredkin gate and MCL gate using less number of qca cell compared to others design. Also represent the layout of URG gate and BJN gate in terms of complexity. During the simulation a consideration is made to reduce the complexity (cell count). The simulation outcome shows that the proposed design, execute well. This paper can further be extended towards the design of higher computing circuit and low power digital circuit in nanotechnology. The proposed layout could be a promising step towards the objective of ultra-low power design in nanotechnology.

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